PATENT SPECIFICATION (11) 1 601 956

1 601 956

(21) Application No. 34412/80 (22) Filed 21 Oct. 1977 (19)

(62) Divided out of No. 1 601 955

(23) Complete Specification filed 2 March 1978

(44) Complete Specification published 4 Nov. 1981

(51) INT. CL.³ G06F 13/00

(52) Index at acceptance

G4A ND

(72) Inventors ARTHUR PHILIP YOUNG,
CLIVE DAVID PURCHASE GILDERSLEEVES,
BRIAN WILLIAM PARTRIDGE
and KEITH LESLIE RYDER

(54) MULTI-PROCESSOR DATA PROCESSING SYSTEMS

(71) We, THE MARCONI COMPANY LIMITED, a British Company, of Marconi House, New Street, Chelmsford, Essex, CM1 1PL, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to data processing systems and in particular to multi-processor data processing systems utilising a data-bus or highway in order to permit the processors in the system to communicate with each other and with memory stores within the system and with external devices.

One example of such a system is the Locus 16 data processing system. "Locus" is a Registered Trade Mark of the Marconi Company Limited.

Usually at least one of the processors in the system is capable of general purpose arithmetic and logical operations using a program stored within the system.

This invention provides a multi-processor data processing system comprising: a store having a plurality of locations each defined by an address; a plurality of processors each having a multi-bit address output and means for feeding at least some bits of this output to the store to provide a corresponding number of bits of an address input of the latter; data transfer means connected between the processors and the store for the communication of data between a processor and an address in the store which address is dependent on the address output of the processor, access control means for controlling access to the store by the processors in response to receipt of a code; a plurality of tables each containing codes; table selecting means for transmitting a processor identity signal indicating what processor is currently to access the store and for selecting a table associated with that processor; means for addressing the selected table with at least part of the address output of that processor which is currently to access the store whereby the table outputs a code; and means for feeding the code outputted by the selected table to the access control means thereby causing said access control means to control acces to the store in a manner defined by said code.

In one form of the invention said multi-bit address output of each processor has A+B digits and means is provided for feeding the B digits to the store to provide a corresponding B digits of said address input of the store; the means for addressing a selected table is adapted to define a table address in dependence on the A digits; each code contained in the tables has Z digits; and said access control means is provided by a further Z digits of said address input of the store and by a connection for feeding the Z digits of the codes outputted by the tables of the corresponding Z digits of the store address whereby said codes limit access of the processors to particular locations in the store.

In another form of the invention the access control means includes means for allowing conditional access, e.g. read only access, to the store.

As will be appreciated, said main store and said table and further stores may be constituted by storage distributed about the system. For example, normally each processor will itself contain registers or other forms of storage which may constitute part of said main store and/or part of said table and/or further stores.

In a practical example A=4 bits, B=12 bits, X=16 bits, Y=20 bits and Z=8 bits.

Preferably all of said stores and said processors are interconnected by a data-bus or highway and, as known *per se* a central control unit is provided to determine which one of said processors is given access to said data-bus at any one time.

Preferably said table store and, where provided, said further store, is accessible for

changing any of the contents thereof to one and one only executive processor. Said last mentioned processor may be one of said plurality of processors or an additional processor.

Each table stored in said table store may relate to data required by an individual one of said processors or to data required by each of a plurality of said processors.

In operation, some or all of said tables relating to data frequently required may be regarded as permanent or resident.

A particular embodiment of the invention will now be described by way of example with reference to Figures 1 and 2 of the accompanying drawings which are highly schematic block diagrams representing two examples of a data processing system in accordance with the present invention, and also in accordance with the invention claimed in our co-pending Application 43908/77. Serial No. 1601955. In both Figures like references are used for like parts.

Referring to Figure 1, twelve processors reference 1 to 12 are connected to a data-bus 13. Also connected to the data-bus 13 is a main store 14, table allocating means constituted by a table store 15, a control unit 16 and an executive processor 17, which constitutes means for changing the table allocating means.

The data-bus 13 is controlled by control unit 16 so as to be capable of passing the following signals:—

(a) Signals from the processors 1 to 12 showing which of these currently awaiting use of the data-bus 13.

(b) Signals from the data-bus control unit 16 indicating which one of the processors 1 to 12 is to make use of the data-bus when this becomes free.

(c) A digital codeword generated by one of the processors 1 to 12 and defining the data item to which access is required by that processor.

(d) A signal defining the nature of the access required, e.g. "read" or "write" and

(e) Signals defining the content of the data item to which access is required, these last mentioned signals being generated by the digital processor currently making use of the data-bus for 'write" operations and being signals generated by the main store 14 or the table store 15 or that one of the digital processors 1 to 12 providing the data for "read" operations.

As known *per se* the data-bus 13 is also provided to carry other types of information such as signals indicating when particular data items are available on the data-bus or when the transfer of particular sets of information is complete or signals relating to the functions of the executive processor 17.

Table store 15 contains twelve tables each individual to a different one of the processors 1 to 12. Each stored table contains a set of addressing codewords relating to different regions of the main store 14. Each of the regions of the main store 14 contains a plurality of data storage areas for individual data items, which may be required by one or more of the processors 1 to 12, at different times.

Each digital processor 1 to 12 is capable of generating a sixteen bit address output. The main store 14 is provided to store of the order of 1,000,000 individual data items at corresponding locations and is capable of being addressed by a 20 bit addressing codeword.

The connection of the table store to the data-bus 13 is such that as the control unit 16 provide access to the data-bus 13 for a particular one of the processors 1 to 12 so, by means of the connection represented at 18 (which constitutes table selecting means) that table in the table store 15 is selected which is appropriate to the particular one of the processors 1 to 12. The addressing 16 bit codeword generated by the particular one of processors 1 to 12 is divided into two parts, the first of which consists of the four most significant digits and the second of which consists of the remaining twelve least significant digits. The four most significant digits are applied to the table store 15 via the connection represented at 19 (which constitutes means for addressing the selected table) to address the selected relevant stored table which thereupon outputs an eight bit codeword which is applied via connection 20 (which constitutes access control means) to the main store 14 to select the region therein which is of interest. The least significant twelve digits of the addressing codeword generated by the selected one of the processors 1 to 12 is applied via data transfer means (constituted by the data-bus and connection 21) to the main store 14 where it is utilised to address the particular region identified in the main store 14 and thus select the data item at that time required by the processor. This is transmitted to the processor via connection 22 and the data-bus 13.

Thus whilst the digital processors are capable of generating sixteen bit addressing codewords only, the effective codeword utilised to address the main store is twenty bits in length and thus the total storage capability of the system is relatively increased. It will be noted that a particular codeword generated by one of the processors 1 to 12 may define the same address in the main store 14 as the identical codeword generated by another of the processors 1 to 12 or it may identify a totally different address as determined by the content of the relevant table in the table store 15.

Whilst in this example a separate executive processor 17 is provided to have exclusive control of the varying or changing of the

tables stored in table store 15, one of the processors 1 to 12 may be designed as an executive processor.

In addition to the twelve tables referred to above, table store 15 also includes storage further defining the permitted nature and extent of the access to the various data items stored in the main store 14. As well as one of the aforementioned addressing codewords being transmitted to address the main store 14, a codeword is also signalled from table store 15 to the main store 14 in order to constrain the response to the addressing of the main store 14 and thus limit the effects of errors in programs.

Referring to Figure 2, again twelve processors reference 1 to 12 are connected to a data-bus 13. Also connected to the data-bus 13 is a main store 14, a table store 15, a control unit 16 and a further or "table number" store 23.

Within table store 15 are stored sixty-four tables relating to data which will be required by the processors 1 to 12. The table store 15 is provided to be addressed via the connection 24 (in this case separate from the data-bus 13 in the interest of speed) by table number store 23. In table number store 23 is stored twelve table numbers each identifying a table within table store 15 which is to be selected when a particular one of the processors 1 to 12 wishing to access the main store 14 is selected. The digital number received from the table number store 23 by the table store 15 to select the appropriate table therein is in six bit form. The addressing of the selected table in table store 15 by the most significant four digits of the addressing codeword generated by the selected processor and the addressing of the selected region of the main store 14 by the least significant twelve digits is as described with reference to Figure 1.

In effect, in both Figures 1 and 2, the tables stored in table store 15 may be considered to provide a plurality of sets of access routes to the different regions of the main store 14, a given set being selected in dependence upon the data required by a particular processor, in the case of Figure 2, as identified by the table number entered into further "table number" store 23.

It will be noted that different processors may at different times access the same table stored in table store 15 and indeed, if the number of different tables required is greater than can be provided in the table store 15, only those tables which are common to more than one of the processors 1 to 12 or which are most commonly in use by one or other of the processors may be stored in the table store 15 in a permanent or resident fashion. Tables relating to less frequently required sets of data items may be replaced in the table store 15 as required.

In addition to the twelve tables referred to in connection with Figure 1 and the sixty-four tables referred to in connection with Figure 2, table store 15 also includes storage further defining the permitted nature and extent of the access to the various data items stored in the main store 14. As well as one of the aforementioned addressing codewords being transmitted to address the main store 14, a codeword is also signalled from table store 15 to the main store 14 in order to constrain the response to the addressing of the main store 14 and thus limit the effects of errors in programs.

WHAT WE CLAIM IS:—

1. A multi-processor data processing system comprising: a store having a plurality of locations each defined by an address; a plurality of processors each having a multi-bit address output and means for feeding at least some bits of this output to the store to provide a corresponding number of bits of an address input of the latter; data transfer means connected between the processors and the store for the communication of data between a processor and an address in the store which address is dependent on the address output of the processor; access control means for controlling access to the store by the processors in response to receipt of a code; a plurality of tables each containing codes; table selecting means for transmitting a processor identity signal indicating what processor is currently to access the store and for selecting a table associated with that processor; means for addressing the selected table with at least part of the address output of that processor which is currently to access the store whereby the table outputs a code; and means for feeding the code outputted by the selected table to the access control means thereby causing said access control means to control access to the store in a manner defined by said code.

2. A multi-processor data processing system in accordance with claim 1 wherein: said multi-bit address output of each processor has A + B digits and means is provided for feeding the B digits to the store to provide a corresponding B digits of said address input of the store; said means for addressing a selected table is adapted to define a table address in dependence on said A digits of said multi-bit address output of each processor; each code contained in the tables has Z digits; and said access control means is provided by a further Z digits of said address input of the store and by a connection for feeding the Z digits of the codes outputted by the tables to the corresponding Z digits of the store address whereby said codes limit access of the processors to particular locations in the store.

3. A multi-processor data processing system in accordance with claim 1 or 2 wherein said access control means includes

means for allowing conditional access, e.g. read only access, to the main store.

4. A multi-processor data processing system in accordance with any preceding claim wherein: each processor has an output on which it produces a processor identification signal identifying itself as being a processor which requires access to the store and said table selecting means includes table allocating means connected to receive the processor identification signal and to select a table which it associates with the processor identified as requiring access.

5. A multi-processor data processing system in accordance with claim 4 wherein there are more tables than processors.

6. A multi-processor data processing system in accordance with claim 5 including means for changing the table allocating means so that it associates different tables with different processors.

ROGER K. TOLFREE,
Chartered Patent Agent,
Marconi House,
New Street,
Chelmsford,
Essex.
Agent for the Applicant.

Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon) Ltd.—1981. Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1601956 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

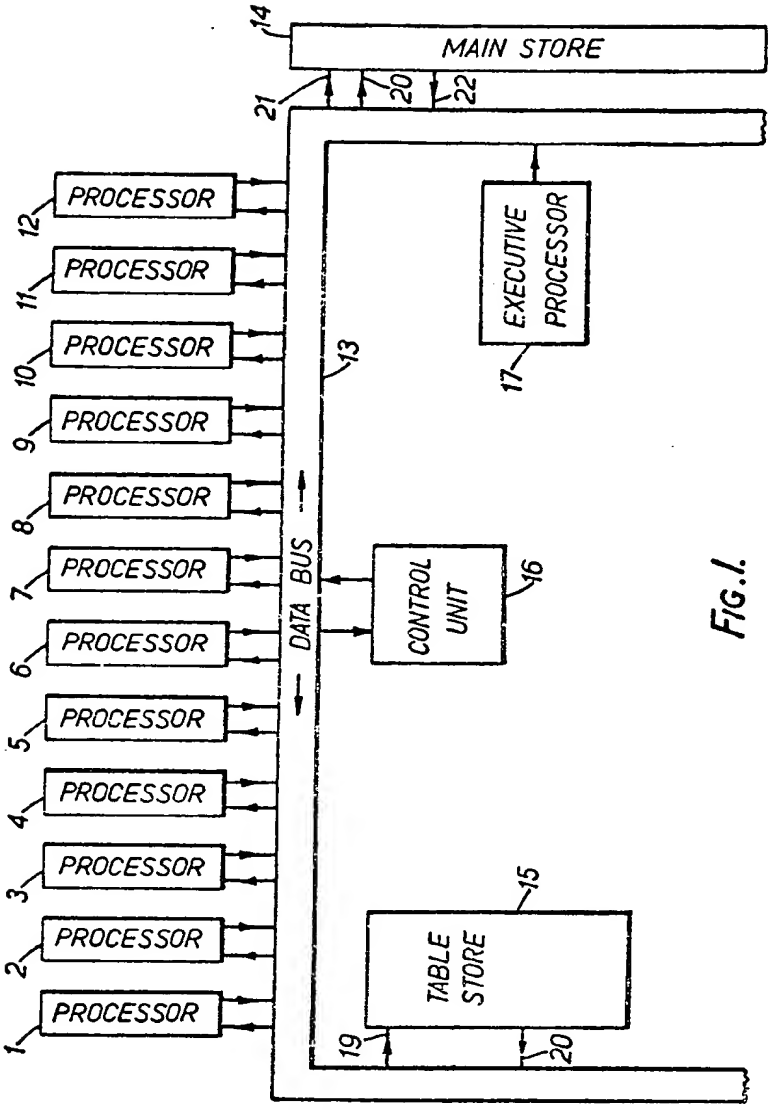

FIG. 1.

1601956 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 2

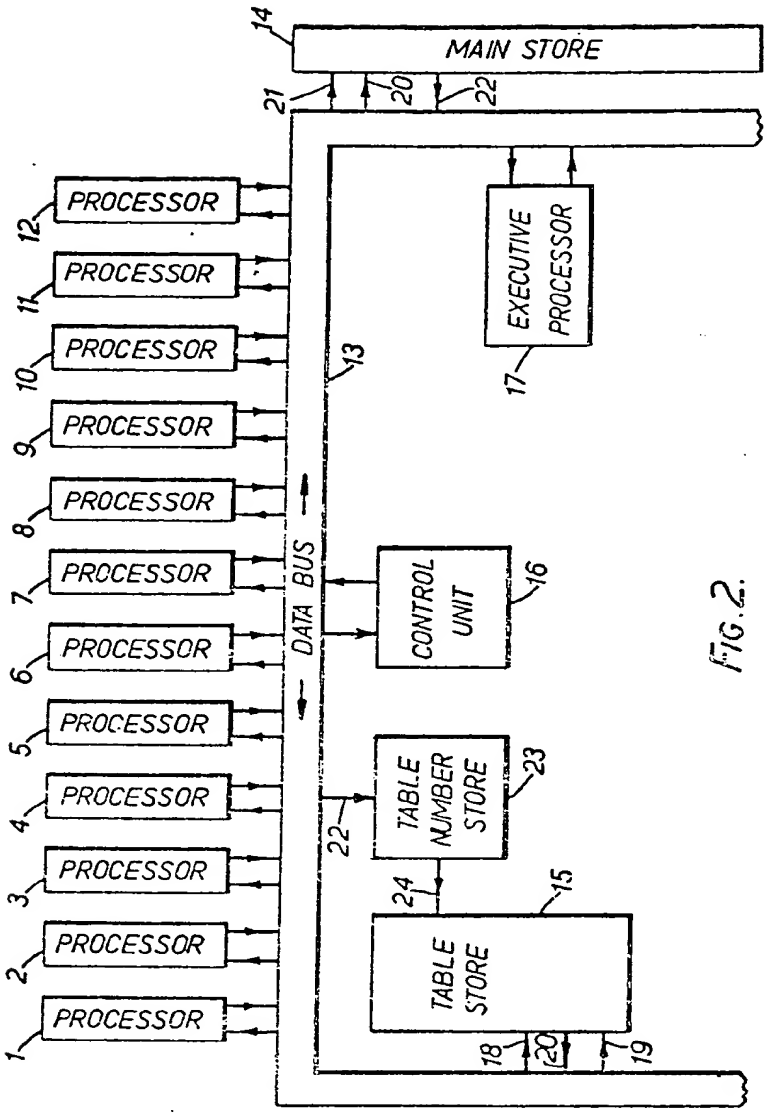

FIG. 2.